

Modeling and Simulation of High Speed Digital Circuits and Interconnects

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Abstract— Careful design, modeling and simulation of modern high speed circuits is a vital issue in today’s electronic industry. High speed data transfer, and high processing power are accomplished if the circuit of the high speed net was modeled and designed properly. We present the main modeling techniques for both high speed circuits and interconnects used in industry nowadays. A modeling example of a 100MHz DDR (Dual Data Rate) memory net is considered. SPICE and IBIS models were used for the drivers/receivers (SSTL), while the interconnects and PCB trace models were generated using a 2D field solver (Maxwell). The net was simulated, and the advantages and disadvantages of various modeling techniques were discussed.

I. INTRODUCTION

High speed computers and communication devices are the most requested electronic equipment in today’s rapidly growing industries. The age of high speed data transfers and processing has begun since the early nineties of last century. Thousands of new electronic innovations have become essential parts of our daily lives. From Personal Computers (PC), Pagers, to PDAs (Personal Digital Assistant) and Cell phones.

In order for a wireless PDA, or a state of the art PC to deliver good and fast data processing, fast application launching, or even good gaming graphics, the need for high speed processing circuits is a vital bottle neck to achieve such performance. The push for more speed and data processing will never end. In the early 1990s, a fast computer with a processor speed of 100MHz was the dream of every computer guru. Nowadays, such speed is not even enough to run a basic program under the windows environment. Such high speed data transfers and processing needs high speed circuits and interconnects to guarantee correct operation and data transmission.

Such high speed circuits and interconnects need to be carefully designed and modeled to give correct system operation. High speed components are connected together via copper trace wires on Printed Circuit Boards (PCB). Also, sometime an external device (i.e. a Hard Drive) needs to get connected to boards, i.e. the PC mother board, this connection is usually done by a connecting cable or connector. Such PCB traces (wires), and connectors are called system interconnects. High speed operation of various components, rises a challenge to the design engineer because alot of frequency dependent parameters starts to appear.

The discipline that is nowadays responsible for such correct high speed communication operation is called *Signal Integrity* (SI). SI engineering, combines Analog/Digital and Electromagnetic theory to analyze high speed circuits and interconnects.

Modeling, Simulation, and Design of high speed circuits needs alot of experience and knowledge. In this paper, we will present the most widely used techniques for high speed modeling and simulation, specially for circuit elements (Drivers/Receivers), and interconnects. In section II we present two well known high speed circuit modeling techniques. Section III touches the area of interconnect modeling. Section IV presents the design, modeling, and simulation of a memory net. Finally we conclude the paper in section V.

II. MODELLING OF HIGH SPEED CIRCUITS

High speed circuit modeling and design is not an easy task. Any chip being developed is separated into various functional blocks, each being developed individually, and then these blocks are glued together (i.e. connected and interfaced) to constitute the whole chip on one die.

Usually the chip designer puts the transistor level architecture for a specific chip (CMOS, LVTTL, GTL, PECL, etc.), and then the chip layout designer makes use of the current technology library to develop the chip. Once the transistor level design is verified and simulated to give the desired performance for the specified technology, a SPICE model for this chip is put (usually the vendor uses his own libraries, so that it can be sold for some extra money), adding to it all the parasitics that was extracted from the chip layout.

Modeling of high speed circuits is usually divided into physical, and behavioral modeling. Physical, is the actual transistor level design of the high speed chip or circuit with all accompanied parasitics. While behavioral deal with the behavior of the circuit when various input/output conditions are encountered. Behavioral modeling is much faster than transistor level modeling, but more accurate results are obtained from physical modeling.

A. Transistor Level modelling (SPICE)

The transistor level design of most chips is done by SPICE. SPICE, stands for *Simulation Program with Inte-*

grated Circuit Emphasis. It is the industry standard for IC design, modeling and simulation. Various vendors provide various versions of SPICE. The most widely used ones in industry are HSPICE (AVANTI Inc.), and KSPICE (CADENCE Inc.), and PSPICE (CADENCE INC., formally ORCAD).

Transistor level modeling is usually complex, specially when the functionality of the circuit increases, and the number of used transistors increase. Current high speed circuits can have more than 1 – *billion* transistors. Usually the simulation of such ICs takes a lot of time, since the analysis will process the state of every single transistor, its operating point, and AC/Transient behavior. Practically, when we model high speed circuits, we tend to focus on the output stage of the driver, which also will constitute of several tens/hundreds of transistors. But simulating such circuit will take much less time than considering the whole architecture of the chip at hand in a chip to chip link.

Simulating drivers and receivers of the current technology, with the desired operation speed, gives a very accurate Signal Integrity analysis if the modeling of drivers/receivers and the interconnects was done accurately. Although transistor level simulations and modeling gives a close to real world circuit behavior, but it usually takes a lot of time to simulate even a single net for several nano-seconds (i.e. an SSTL¹ memory net takes about 3 hours to simulate on a super computer (32-Processors) for 100nsec).

B. Behavioral modelling (IBIS)

IBIS is an acronym for *I/O (Input-Output) Buffer Information Specification*. It is a template (standard, data-exchange format, etc.) for exchanging modeling information between semiconductor device suppliers, simulation software suppliers and end users.

IBIS models are not models in the more traditional meanings of that word where a modeling language and/or schematic symbol, and/or n^{th} -order polynomial representation of a device and/or its internal structure is being represented. Such models are referred to as physical models because the physical elements are being described. But, the IBIS model is a model in the sense that the behavior of a device is being represented. The radical departure for IBIS is to catalog the output and input behaviors of devices in the form of curves, or actually, tables of data that catalog how an output or input behave electrically. [4]

IBIS modeling includes the V-I (voltage-current) and V-T (voltage-time) curves representing the behavior of the chip modeled, it also includes the various parasitics of input/output, VCC, and GND pins. It might include the coupling between pins, to simulate and represent any crosstalk behavior and such. Newer versions even consider differential nets and their respective behavior. Figures 1 and 2 show an IBIS Input model for a receiver, and the

IBIS output model of a driver respectively.

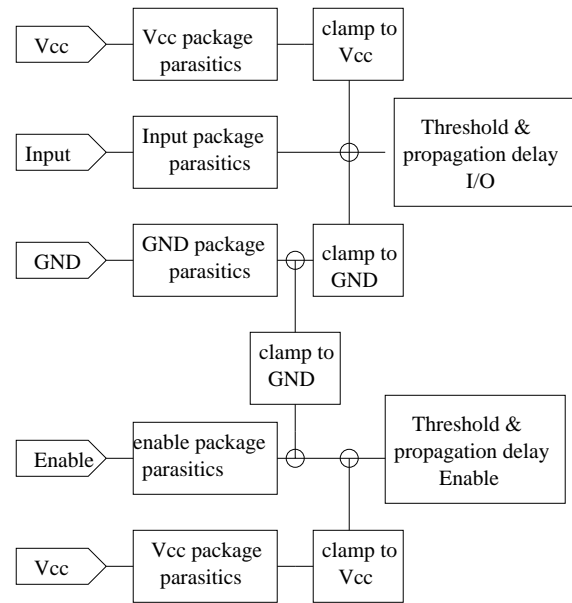


Fig. 1. IBIS receiver/Input model.

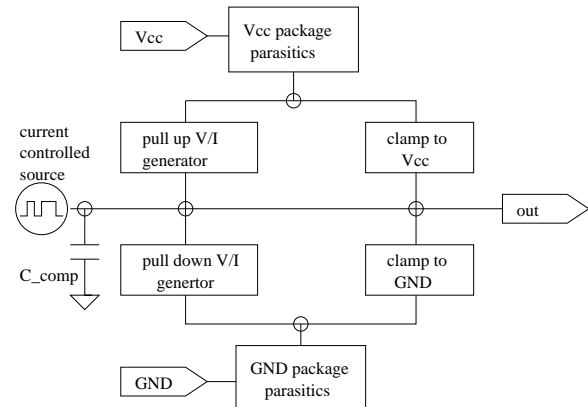


Fig. 2. IBIS driver/Output model.

The figures show that the models consist of various tables that describe the behavior of the component to various input/output signal levels. Also, it includes the parasitics incorporated in the V_{cc} and GND pins, as well as the input/output pins.

Behavioral modeling has proven to be much faster in simulating the behavior of a high speed net than physical modeling that gives you the transistor level structure of any driver/receiver. Actual simulations have proven that behavioral IBIS modeling is at least 10 times faster than a SPICE based model. So, this makes such kind of modeling very appealing, specially when we consider simulating large amounts of nets which might take days to accomplish if represented via physical models on a supercomputer. A major drawback of IBIS modeling is that it is not as mature as physical models that are being supplied by all IC vendors. These days, most of the new components are being manufactured with their SPICE and IBIS models delivered

¹Stub-Series Terminated Logic

to circuit and board designers.

Usually IBIS models are generated by actually simulating physical SPICE models, and then extracting the V-I, and V-T curves with any accompanied parasitics added to the model. Or, sometimes, such curves are being tabulated from lab measurements for the specified IC. There are some tools that can be used to generate IBIS models from SPICE models, and a free tool from the *University of North Carolina* was used in one of the simulations conducted in the coming sections.

III. MODELLING OF INTERCONNECTS

Interconnect modeling for high speed circuits is very important. Since at high speeds a PCB trace is no longer considered as a lumped RC (resistor-capacitor) network, this trace behaves like a transmission line. Such a transmission line has parameters like characteristic impedance (\mathbf{Z}_o), propagation delay (\mathbf{TD}), attenuation constant (α), and various other parameters that degrade the signal quality, and adds some delay on signal transmission.

$$\mathbf{Z}_o = \sqrt{\frac{L}{C}} \quad \mathbf{TD} = \sqrt{LC} \quad (1)$$

$$\alpha = \exp\left[\frac{-Rl}{2\mathbf{Z}_o}\right] \quad (2)$$

where L , C , R , l , and \mathbf{Z}_o are the inductance, capacitance, resistance, length, and characteristic impedance of the trace respectively.

In high speed circuit modeling and design, PCB traces, along with connector models that usually connect a daughter board to a mother board, or connects a cable to the board, along with via models that represent the behavior of a discontinuity in the signal path as it travels from one layer on the PCB to another, all these should be modeled carefully to accurately represent the behavior of the circuit at a specified range of frequencies, to get an accurate model, and design, and get the circuit operating after receiving the board from the fabrication house.

A. PCB Trace modelling

To accurately model PCB traces, a designer needs to make use of 2D or 3D electromagnetic field solvers. The topology of the trace to be used in the design is passed to the field solver, to accurately model the parameters of the traces to be used in the design. Fig. 3 shows a 2D cross section of a 3 conductor stripline PCB. The trace can be simulated and modeled with various geometries to give the designer the behavior needed, and then the resulting parameters are passed to the circuit/interconnect simulator to test the trace with other net parts.

MAXWELL is a 2D/3D field solver from Ansoft Inc. In the tool, the designer draws the geometry of the traces, the separation, the dielectric constant of the stripline/microstrip transmission line, and the frequency of operation, to get the RLGC matrices for such a PCB topology. In addition, this tool gives the frequency dependent

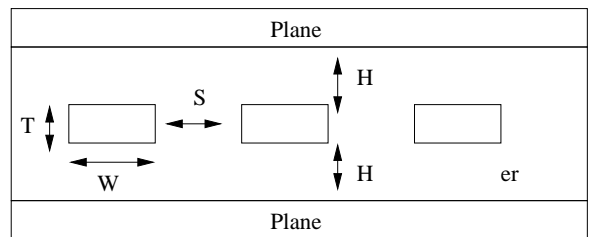


Fig. 3. A 3-conductor PCB cross-section. Stripline.

parameters of such traces, like the skin effect, and dielectric losses. This will yield an accurate modeling of such an interconnect. The resulting matrices, that describe self and mutual effects, are put in a file than can be incorporated into your SPICE code, and can be simulated as a transmission line via the $w - line$ command.

B. Connector and Via models

Connectors are used to connect boards together, or to connect cables to boards. There are so many types of connectors based on the applications, and the standards used in the design. Connector types vary from the well know Edge Connectors that are used to connect daughter boards like a PCI (Peripheral Component Interconnect) card to the PC mother board, to AGP (Accelerated Graphics Port) connectors that connects high speed AGP boards to mother boards, to the very high speed ($250MHz <$) Meg-array connectors that are in BGA (Ball Grid Array) shapes [13]. The modeling of such connectors is very important to get the correct signal behavior at the other end of the net. Connectors are discontinuities in the signal path, and they should be carefully modeled. Usually, the company delivering the connector characterizes the behavior of its design, and delivers the SPICE file representing its behavior for board designers.

Vias are being obtained when a trace net is routed on one layer, and then continued on another. The drill in the board that causes this net to change layers is called a via. Vias do affect the signal flow since they represent a discontinuity in the signal path with a different (\mathbf{Z}_o) and (\mathbf{PD}). Via behavior is usually extracted from board tools (Pacific Numerics (PNC) from Ansoft Inc, or SpecctraQuest (SQ) from Cadence Inc.), and back substituted in simulation programs to compare the modeling effect with actual. The via model depends on the geometry of the drill, and the stackup of the board.

Fig. 4 shows an Edge connector and via models. These models are used in the simulations considered in the following section. Such values are taken from the DDR (Dual Data Rate) DRAM (Dynamic Random Access Memory) specification [7], [8].

IV. MODELLING EXAMPLE

In this section we model and simulate a memory net using transistor level and behavioral modeling techniques. The net simulated is a 100MHz DDR memory net (200Mbps). The net is being driven by a bridge chip, and the DRAM receiver is on the DIMM (Dual In-line Main

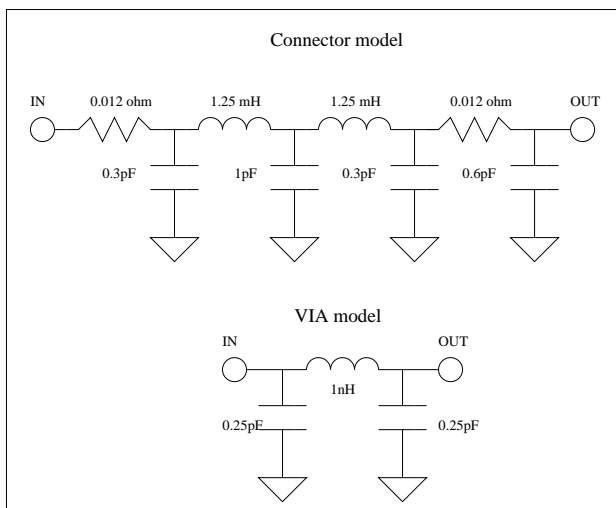


Fig. 4. Connector and Via models used in simulations and taken from [7].

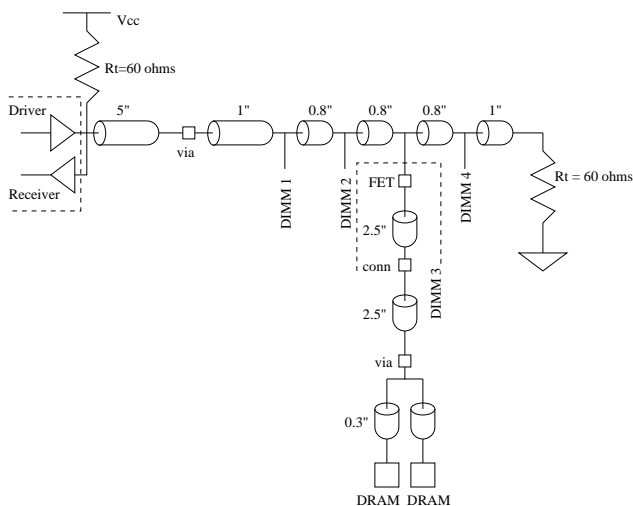


Fig. 5. Topology of memory net simulated.

Memory) board. It is assumed that only one DIMM is active at a time, this is a real world case. The net topology is shown in Fig. 5. The net is driven by an IBM SSTL2 driver. The driver SPICE model is used in one simulation, and then we generated the IBIS model of this driver using the SPARTAN tool from *UNC* [12]. The load on the DIMM was a capacitor of $2pF$. DIMM 3 was the activated one in the simulations.

The lengths of the traces shown in Fig. 5 are, $L_1 = 5''$, $L_2 = 1''$, $R_t = 60\Omega$, $Z_0 = 60\Omega$, $L_p = 0.8''$, $L_t = 1.0''$.

The IBIS model result is shown in Fig. 6. While the SPICE model result is shown in Fig. 7. The IBIS model used for the SSTL2 driver/receiver was added to the memory net and simulated using the SQ tool. The SPICE SSTL2 driver/receiver model was added to the SPICE deck, and simulated using HSPICE.

The results show that the behavior of the nets is close. There is non-monotonic behavior on the dram inputs when DIMM 3 is active (we chose DIMM3 because the amount of reflections is worse for this DIMM because of its location on the net). The amount of reflection and non-monotonic

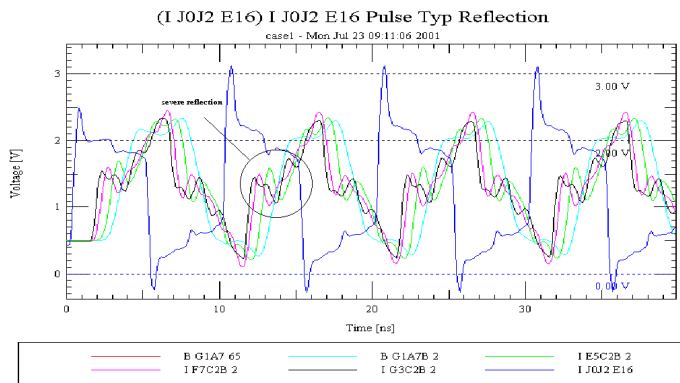


Fig. 6. The result when using the IBIS model, and DIMM 3 is loaded.

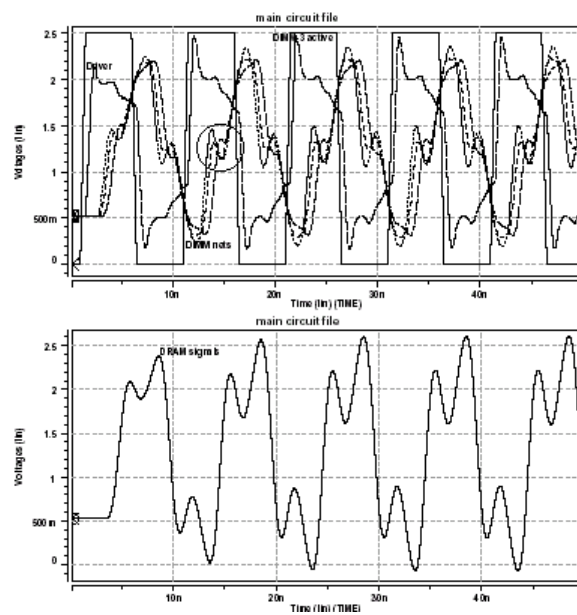


Fig. 7. The result obtained when using the SPICE model, and DIMM 3 is loaded.

behavior is obvious in both simulations. The IBIS model simulation suffers from a more severe behavior, note that the overshoot at the driver side exceeds the SPICE one by about 0.5V. This is due to the fact that the V-I and V-T curves in the IBIS model have limited behavior, and cannot supply the same amount of accuracy as the original transistor level simulation. While the level at the receiver side (which is what actually matters) is close to that of the SPICE simulation. Usually, IBIS simulations give us an indication whether the net topology will perform in an acceptable manner or not. These days, IBIS modeling is becoming more and more widely used, and the resulting simulations are even closer to SPICE ones. Off-course the trade between speed of simulation and accuracy is always there.

The second waveform in the SPICE simulation result shows the shape of the wave at the input of the DRAM. The behavior is acceptable with good margin since the threshold is about 1.25V.

V. CONCLUSIONS

High speed circuit design is one of the most important aspects in today's electronics industry. At high frequencies, careful modeling of circuits and interconnects should be performed. We have presented the features of physical versus behavioral circuit modeling. We have illustrated the IBIS and SPICE circuit modeling techniques. The generation of high speed trace models using field solvers is very important to include high frequency effects in the design model. Maxwell is the industry used field solver for such trace modeling tasks. We illustrate the modeling of such high speed circuits and interconnects via a DDR memory net running at 100MHz. Behavioral modeling is faster to simulate and characterize than physical models, but there is an accuracy trade off.

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